REMARKS/ARGUMENTS

In the Office Action mailed June 24, 2010, claims 1 and 3-24 were rejected. In response, Applicants hereby request reconsideration of the application in view of the below-provided remarks. No claims are amended, added, or canceled.

Claim Rejections under 35 U.S.C. 103

Claims 1 and 3-24 were rejected based on one or more cited references. The cited reference(s) relied on in these rejections include:

Churchill et al. (U.S. Pat. No. 6,115,836, hereinafter Churchill)
Irrinki et al. (U.S. Pat. No. 5,822,228, hereinafter Irrinki)
Savir (U.S. Pat. No. 5,642,362, hereinafter Savir)
Lackey (U.S. Pat. No. 6,467,044, hereinafter Lackey)
Choi (U.S. Pat. No. 6,324,115, hereinafter Choi)

In particular, claims 1, 3-13, and 16-20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill in view of Irrinki, Savir, and Lackey. Claims 14, 15, and 21-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill, Irrinki, Savir, and Lackey in view of Choi. However, Applicants respectfully submit that these claims are patentable over Churchill, Irrinki, Savir, Lackey, and Choi for the reasons provided below.

Independent Claim 1

Claim 1 is patentable over the combination of Churchill, Irrinki, Savir, and Lackey because the combination of cited references does not teach all of the limitations of the claims. Moreover, the proposed combination of cited references is improper because Lackey teaches away from the proposed combination with Churchill. Claim 1 recites:

A method comprising:

receiving an internal clock signal from a clock monitor of the self-timed memory;

receiving an external clock signal, wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal;

receiving a control signal;

providing, in dependence upon the control signal, the internal clock signal to at least one internal memory block during a normal mode of operation of the self-timed memory, and the external clock signal to the at least one internal memory block during a test mode of the self-timed memory, wherein providing the external clock signal to the at least one internal memory block comprises providing the external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern; and

detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test-mode of the self-timed memory.

(Emphasis added.)

In contrast to the language of the claim, the combination of Churchill, Irrinki, Savir, and Lackey does not teach all of the limitations of the claim. In particular, the combination of cited references does not teach providing an external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern. Furthermore, the asserted combination of the teachings of Lackey with Churchill is improper because Lackey specifically teaches away from the use of an external clock signal.

1. The combination of cited references does not teach providing an external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern.

Despite the assertions in the Office Action, the combination of cited references does not teach providing an external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern. For reference, the Office Action acknowledges that Churchill does not teach the indicated limitation. Office Action, 6/24/10, page 3 ("Churchill does not explicitly teach…a predetermined test pattern to provide the external clock signal."). The reasoning in the Office Action does

not assert that Irrinki or Savir might teach the indicated limitation. Hence, the reasoning in the Office Action relies on Lackey as purportedly teaching functionality to provide an external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern. Office Action, 6/24/10, page 4 (with reference to col. 5, lines 61-65, and col. 6, lines 10-16, of Lackey).

However, Lackey does not teach an external clock. Lackey merely teaches a clocking architecture that uses a single internal system clock to generate multiple clock domains for test operations. Lackey, col. 3, lines 32-42; Fig. 1, system clock 10. The system clock is not an external clock. Moreover, Lackey does not illustrate or teach using any type of external clock within the clocking architecture.

Given that Lackey does not describe an external clock, Lackey also fails to describe providing an external clock to different internal memory blocks according to a predetermined test pattern. Therefore, the asserted combination of cited references does not teach all of the limitations of the claim at least because Lackey does not teach providing an external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern.

2. Lackey teaches away from using an external clock signal.

Despite the Examiner's attempt to combine the teaching of Lackey with Churchill, Lackey teaches away from systems which use an external clock. Within the context of a 103 rejection, MPEP 2141 recognizes three factual inquiries that should be analyzed:

1. Determine the scope and content of the prior art;
2. Ascertain the differences between the claimed invention and the prior art; and
3. Resolve the level of ordinary skill in the art.

In ascertaining the differences between the claimed invention and the prior art (factual inquiry #2), the MPEP further states that "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." MPEP 2141.02(VI) (emphasis in original) (citing *W.L. Gore &*

Associates, Inc. v. Garlock, Inc., 721 F.2d 1540 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). The MPEP also recognizes that "the prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." Id. (quoting *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). Thus, the description of a mere alternative embodiment is not necessarily a teaching away if the alternative embodiment is not criticized, discredited, or otherwise discouraged. Conversely, the Federal Circuit explained "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference..." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 132y (Fed. Cir. 2009) (emphasis added) (quoting *Ricoh Co., Ltd. v. Quanta Computer Inc.*, 550 F.3d 1325, 1332 (Fed. Cir. 2008) (further quoting *In re Kahn*, 441 F.3d 977, 990 (Fed. Cir. 2006))). Thus, a reference teaches away if it discourages the teaching.

In the present case, Lackey teaches away from the use of multiple clocks from different clock domains that do not operate synchronously with each other. Lackey, col. 2, lines 7-13. One of the problems associated with using such multiple clock domains is that additional data path lock is necessary to synchronize the different domain paths, which results in unwanted cost of circuit area, logic design complexity, and performance impact. Lackey, col. 2, lines 15-19. Another of the problems associated with using such multiple clock domains is the blocking of the multiple paths, which results in loss of test coverage, as well as cost of circuit area, logic design complexity, and performance impact. Thus, Lackey identifies specific disadvantages that discourage the use of an external clock or any other type of asynchronous clock domain.

An external clock is necessarily asynchronous and in a different clock domain relative to an internal system clock. Thus, the use of an external clock would be subject to all of the same disadvantages that Lackey outlines. The implication of these disadvantages is that Lackey clearly discourages the use of external clocks, just like any other clock that is asynchronous and operates in a different clock domain. Apparently the design proposed in Lackey is intended to address these problems by specifically deriving different internal clock domains from a single system clock.

These descriptions in Lackey not only point out some of the perceived disadvantages of using external clocks and other asynchronous clock domains, but Lackey generally characterizes these implementations as having problems and associated costs, which indicates that Lackey discourages using such implementations. Thus, Lackey discourages using external clocks and other asynchronous clock domains.

Moreover, *DePuy* further states "An inference of nonobviousness is especially strong where the prior art's teachings undermine the very reason being proffered as to why a person of ordinary skill would have combined the known elements." *DePuy* at 1326. Here, the reasoning in the Office Action states that the problems identified in Lackey (using asynchronous clock domains in testing) are supposedly the basis for one skilled in the art to combine the teachings of Lackey with Churchill. The characterization of asynchronous clock domains as a problem in Lackey undermines the Examiner's assertion that implementing an external clock in Lackey might be an advantage of the combination of Lackey and Churchill.

For these reasons, the proposed combination of Lackey and Churchill is improper because Lackey teaches away from using an external clock. Accordingly, Applicants respectfully request that the asserted rejections be withdrawn because Lackey teaches away from the proposed combinations of cited references.

Independent Claims 9 and 17

Applicants respectfully assert independent claims 9 and 17 are patentable over the proposed combination of cited references at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Each of these claims recites subject matter which is similar to the subject matter of claim 1 discussed above. Although the language of these claims differs from the language of claim 1, and the scope of each claim should be interpreted independently of other claims, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejections of these claims.

Dependent Claims

Claims 2-8, 10-16, and 18-24 depend from and incorporate all of the limitations of the corresponding independent claims 1, 9, and 17. Applicants respectfully assert these dependent claims are allowable based on allowable base claims. Additionally, each of these dependent claims may be allowable for further reasons.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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